We claim:

Sub a2

1. A method performed in an error correction system, the method comprising the steps of:

determining if an actual number of errors is less than a maximum error correction capability; and

reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability.

2. The method of claim 1, wherein the step of reducing power consumption further comprises the step of gating one or more clocks coupled to the error correction system.

3. The method of claim 1, further comprising the step of providing a plurality of intermediate polynomials, and wherein the step of reducing power consumption in the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree.

4. The method of claim 3, wherein one intermediate polynomial is $R(x)$, wherein one intermediate polynomial is $F(x)$, wherein one intermediate polynomial is $Q(x)$, wherein one intermediate polynomial is $G(x)$, and wherein the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree further comprises the step of determining if a degree of either $R(x)$ or $Q(x)$ is less than a predetermined degree.

5. The method of claim 3, further comprising the step of providing, in the decoder, a plurality of intermediate polynomial elements and a calculation circuit coupled to the intermediate polynomial elements, each intermediate polynomial element containing coefficients of one of the intermediate polynomials, and wherein the step of reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of placing a predetermined state

into each of the intermediate polynomials, the predetermined state selected to reduce switching of the calculation circuit.

6. The method of claim 5, wherein the predetermined state is zero.

7. The method of claim 1, further comprising the steps of:
determining a plurality of syndromes;
determining if all of the syndromes have a predetermined value; and
reducing power consumption of the decoder of the error correction system when all of the syndromes have the predetermined value.

8. The method of claim 7, wherein the predetermined value for each syndrome is zero.

9. The method of claim 7, wherein the method further comprises the steps of providing a key equation solving device in the decoder, and providing a plurality of syndrome generators, each of the syndrome generators determining one of the syndromes, wherein the key equation solving device is coupled to each of the syndrome generators, and wherein the step of reducing power consumption of the decoder of the error correction system when all syndromes have the predetermined value further comprises the step of not enabling the key equation solving device when all of the syndromes have the predetermined value.

10. The method of claim 9, further comprising the step of calculating at least one error polynomial when at least one syndrome does not have the predetermined value.

11. A decoder comprising:
a key equation determination device comprising:
a plurality of registers, each register adapted to hold coefficients of an intermediate polynomial;

a calculation circuit adapted to calculate new values of the coefficients in the registers in order to determine two error polynomials; and

a control circuit coupled to at least one of the registers, the control circuit adapted to determine when an actual number of errors is less than a maximum error correction capability and to place the calculation circuit into a low power mode when the actual number of errors is less than the maximum error correction capability, the control circuit using at least one of the registers when determining the actual number of errors.

12. The decoder of claim 11, wherein for the key equation determination device:

the plurality of registers are four registers;

the control circuit determines when an actual number of errors is less than a maximum error correction capability by determining if a degree of at least one of polynomials that correspond to a register is less than a predetermined degree; and

the control circuit places the calculation circuit into a low power configuration by providing predetermined inputs to the registers.

13. The decoder of claim 12, wherein for the key equation determination device:

the predetermined inputs are zeros;

each register holds coefficients for one of a polynomial $R(x)$, a polynomial $F(x)$, a polynomial $Q(x)$, and a polynomial $G(x)$; and

the key equation determination device further comprises four operating modes, a first mode that is performed by the calculation circuit and that calculates new values of the coefficients in the registers in order to determine two error polynomials, a second mode that reduces a degree of $R(x)$, a third mode that reduces a degree of $Q(x)$, and a fourth mode that inputs zeros to the registers.

14. The decoder of claim 13, wherein:

the key equation determination device further comprises four multiplexers;

the key equation determination device further comprises three additional circuits that are coupled to outputs of the registers and to inputs of the four multiplexers;

each of the second, third, and fourth operating modes is performed by one of the additional circuits;

the calculation circuit and the three additional circuits operate in parallel;

outputs of the multiplexers are coupled to inputs of the registers; and

the control circuit selects, during each cycle, an output of one of the four multiplexers, thereby selecting an output of one of the operating modes.

15. The decoder of claim 14, wherein the control circuit selects an output of the mode according to the following:

the output of the first mode when both a leading coefficient of $R(x)$ and a leading coefficient of $Q(x)$ are nonzero;

the output of the second mode when the leading coefficient of $R(x)$ is zero;

the output of the third mode when the leading coefficient of $Q(x)$ is zero; and

the output of the fourth mode when the degree of $R(x)$ is less than a predetermined value or when the degree of $Q(x)$ is less than a predetermined value.

16. The decoder of claim 11 further comprising:

a plurality of syndrome generators coupled to the key equation determination device, each syndrome generator generating a syndrome in a predetermined number of cycles; and

wherein the key equation determination device accepts a syndrome from each of the syndrome generators and determines the two error polynomials for each syndrome, wherein the key equation determination device is capable of determining all of the error polynomials for all of the syndrome generators during a number of cycles that is less than the predetermined number of cycles.

17. The decoder of claim 16, further comprising a syndrome buffer placed between and coupled to the plurality of syndrome generators and the key equation determination device, the syndrome buffer accepting each syndrome.

18. The decoder of claim 17, further comprising a second control circuit, the second control circuit coupled to the syndrome buffer and to the control circuit of the key equation determination device through at least one control signal, the second control circuit operating the at least one control signal to cause one of the syndromes in the syndrome buffer to be transferred to the key equation determination device and to cause the key equation determination device to determine the two error polynomials for the one syndrome, wherein each of the syndromes are serially transferred to the key equation determination device.

19. The decoder of claim 16, further comprising:

a syndrome testing device, the syndrome testing device testing all of the syndromes to determine if each syndrome has a predetermined value; and

a second control circuit coupled to the syndrome testing device and to the control circuit of the key equation determination device, the second control circuit placing the key equation determination device in a low power configuration when all syndromes have the predetermined value.

20. The decoder of claim 19, wherein the predetermined value for each syndrome is zero.

21. The decoder of claim 19, wherein the second control circuit comprises a control signal coupled to the control circuit of the key equation determination device, and wherein the second control circuit places the key equation determination device in low power configuration by placing the control signal in predetermined state wherein the key equation determination device does not perform calculations to determine the at least one error polynomial.

22. The decoder of claim 19, wherein the second control circuit comprises first and second portions, wherein the first portion is coupled to the syndrome testing device and to the second portion, and wherein the second portion is coupled to the control circuit of the key equation determination device, the first portion directing the second portion to place the key equation determination device in the low power configuration when each syndrome is the predetermined value.

23. A decoder comprising:

means for determining a key equation, comprising:

a plurality of registers, each register adapted to hold coefficients of an intermediate polynomial;

means for calculating new values of the coefficients in the registers in order to determine two error polynomials; and

means for determining when an actual number of errors is less than a maximum error correction capability and to place the means for calculating into a low power mode when the actual number of errors is less than the maximum error correction capability, the means for determining using at least one of the registers when determining the actual number of errors.

24. The decoder of claim 23, further comprising:

a plurality of syndrome generators coupled to means for determining the key equation, each syndrome generator generating a syndrome in a predetermined number of cycles; and

wherein the means for determining a key equation accepts a syndrome from each of the syndrome generators and determines the two error polynomials for each syndrome, wherein the means for determining a key equation is capable of determining all of the error polynomials for all of the syndrome generators during a number of cycles that is less than the predetermined number of cycles.

25. A decoder comprising:

means for determining if an actual number of errors is less than a maximum error correction capability; and

means for reducing power consumption in a decoder of an error correction system when the actual number of errors is less than the maximum error correction capability.

26. An integrated circuit comprising:

means for determining if an actual number of errors is less than a maximum error correction capability; and

means for reducing power consumption in a decoder of an error correction system when the actual number of errors is less than the maximum error correction capability.

27. An encoder adapted to accept a first, a second, and a third input per cycle, the encoder comprising:

a three-parallel encoder adapted to accept a first, a second, and a third three-parallel input per cycle and adapted to determine a plurality of redundant output symbols after a predetermined number of cycles;

a circuit adapted to place a zero on the first three-parallel input during a first cycle of the three-parallel encoder and adapted to input zeros to the first, second, and third three-parallel inputs after a second predetermined number of cycles;

a first delay element coupled to the third input, an output of the first delay element coupled to the third three-parallel input;

a first additional delay element coupled to the second three-parallel input;

a second additional delay element coupled to the third three-parallel input; and

wherein the first input is coupled to the second three-parallel input and the second input is coupled to the third three-parallel input, and wherein the first, second, and third inputs are output by the encoder one cycle after being input to the encoder.